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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,909	08/12/2004	Brent A. Anderson	BUR920040109US1	7952
30449	7590	04/27/2005		EXAMINER
SCHMEISER, OLSEN + WATTS			DANG, PHUC T	
3 LEAR JET LANE			ART UNIT	PAPER NUMBER
SUITE 201				
LATHAM, NY 12110			2818	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/710,909	ANDERSON ET AL. <i>(CH)</i>
	Examiner	Art Unit
	PHUC T. DANG	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on election on March 24, 2005.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 1-16 is/are allowed.
 6) Claim(s) 17-20 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 12 August 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 081204.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

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DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I (claims 1-16) filed on March 24, 2005 has been acknowledged.

Restriction filed on March 2, 2005 has been withdrawn as requested by the Applicant's election discussed above.

Claims 1-20 are currently pending in the application for examining at this time.

Oath/Declaration

2. The oath/declaration filed on August 12, 2004 is acceptable.

Information Disclosure Statement

3. The office acknowledges receipt of the following items from the applicant:

Information Disclosure Statement (IDS) filed on August 12, 2004.

Specification

4. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was

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commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 17-18 and 20 are rejected under 35 U.S.C. 102 (e) as being anticipated by Guo (U.S. Publication No. US 2003/0211684 A1).

Regarding claim 17, Guo discloses a semiconductor structure, comprising:

- (a) a semiconductor channel region (Figs. 1-7),
- (b) a gate dielectric region (52, Fig. 7) being on top of the semiconductor channel region;
- (c) a gate region (54 & 56, Fig. 7) being on top of the gate dielectric region (52, Fig. 7)

and being electrically isolated from the semiconductor channel region (54 & 56, Fig. 7) by the gate dielectric region (52, Fig. 7), and

(d) first and second gate dielectric side plates (66, Fig. 7) being on top of the gate dielectric region (52, Fig. 7) and being on side walls of the gate region (54 & 56, Fig. 7), wherein the gate region (54 & 56, Fig. 7) is sandwiched between first and second gate dielectric side plates (66, Fig. 7), and

wherein a top surface of the gate region (54 & 56, Fig. 7) is lower than top surfaces of the first and second gate dielectric side plates (66, Fig. 7).

Regarding claim 18, Guo discloses the first and second gate dielectric side plates comprise a low-K material [[0084] page 5].

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Regarding claim 20, Guo discloses the entire gate region (54 & 56, Figs. 2-3) is at a higher level than the semiconductor channel region.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guo in view of Dakshina-Murthy et al., hereinafter “Dakshina-Murthy” (U.S. Patent No. 6,855,582 B1).

Guo discloses all the features of the claimed invention as discussed above, but does not discloses the semiconductor channel region comprises a fin region formed on top of a buried dielectric layer.

Dakshina-Murthy, however, discloses the semiconductor channel region comprises a fin region formed on top of a buried dielectric layer [Figs. 1A-1B and col. 4, lines 4-9].

It would have been obvious to one having ordinary skilled in the art at the time the invention was made to apply the teaching of Dakshina-Murthy to Guo discussed above such that the semiconductor channel region comprises a fin region formed on top of a buried dielectric layer for a purpose of reducing source/drain parasitics [col. 7, lines 8-10]..

Allowable Subject Matter

7. Claims 1-16 would be allowed.

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The following is a statement of reason for the indication of allowable subject matter:

Claims 1-16 are considered allowable since the prior art of record and the considered pertinent to the applicant's disclosure does not teach or suggest the claimed invention having a step of (c) forming a gate stack on top of the gate dielectric layer, wherein the gate stack is electrically isolated from the semiconductor channel region by the gate dielectric layer, wherein the gate stack comprises (i) a gate region on top of the gate dielectric layer, and (ii) a gate stack mask on top of the gate region, wherein the gate stack mask comprises a gate mandrel and first and second gate spacers, and wherein the gate mandrel is sandwiched between the first and second gate spacers as cited in claims 1 and 14.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and After Final communications.

10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

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Phuc T. Dang

FD



Primary Examiner

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